SSL5301T

Mains dimmable controller for LED lighting

Rev. 2 — 30 June 2014 Product data sheet

1. General description

The SSL5301T is a mains dimmable controller IC, intended to drive dimmable LEDs in general lighting applications.

The main benefits of this IC include:

- High dimmer compatibility
- Selectable modes for high power factor or low ripple, allowing a wide LED power range
- Large dimming range
- Single stage topology for small PCB footprint
- Ease of design-in
- Integrated start-up JFET
- Low electronic Bill Of Material (BOM)
- Supports multi-lamp applications
- Various converter topologies supported

The IC drives an external switch for easy power scaling. It has been designed to start up directly from the High-Voltage (HV) supply by an internal high-voltage current source. Flyback, buck and buck-boost circuit topologies are supported. Primary side sensing provides accurate output current control.

The IC can detect all known mains dimmer types and translate the dimmer setting to a continuous LED current in multiple ways. It can operate in three switching modes at two switching frequency ranges. It offers tradeoffs between the output current ripple, the mains current Total Harmonic Distortion (THD) and the application size. The IC incorporates all required protection features.

2. Features and benefits

- LED controller IC for driving strings of LEDs or high-voltage LEDs from rectified mains
- High-efficiency switch mode buck, flyback or buck-boost controller driving an external power FET
  - Two maximum switching frequencies for highest efficiency or smallest application size
  - Zero current switching at switch turn-on
  - Zero voltage or valley switching at switch turn-on
  - Selectable low THD or low LED current ripple modes

- Leading, trailing and intelligent dimmer detection
- Two built-in dim curves
- LED current accuracy within ±4 % across variations in components and conditions
- No binning on LED forward voltage required
- Built-in Protections:
  - UnderVoltage LockOut (UVLO)
  - Leading Edge Blanking (LEB)
  - OverCurrent Protection (OCP)
  - Internal OverTemperature Protection (OTP)
  - Brownout protection
  - Output Short Protection (OSP)
  - Output open OverVoltage Protection (OVP)
  - Mains synchronization loss protection
  - Bleeder dissipation protection
- Low component count LED driver solution
- Compatible with wall switches with built-in indication light during standby
- Operates well in multiple-lamp arrangements
- IC lifetime matches or surpasses LED lamp lifetime

3. Applications

- Compact mains dimmable LED lamps with accurate, dimmable current output for single mains voltages, including 100 V (AC), 120 V (AC) and 230 V (AC). External components determine the power level. The power level ranges from 4 W to over 25 W. Applications fit in common form factors like PAR, GU10, A19, and the candle form factor.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		8.8	-	32	V
f_{sw}	switching frequency	low-frequency mode; undimmed				
		50 Hz mains	55	60	65	kHz
		60 Hz mains	66	72	78	kHz
		high-frequency mode; undimmed				
		50 Hz mains	84	91	98	kHz
		60 Hz mains	101	109	117	kHz
I_{CC}	supply current	normal operation	-	2.25	-	mA
$V_{I(DRAIN)}$	input voltage on pin DRAIN	not repetitive	-	-	700	V
$V_{o(PWRDRV)}$	output voltage on pin PWRDRV	high level	-	10.7	-	V

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5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SSL5301T	SO8	plastic small package outline body; 8 leads; body width 3.9 mm	SOT96-1

6. Block diagram

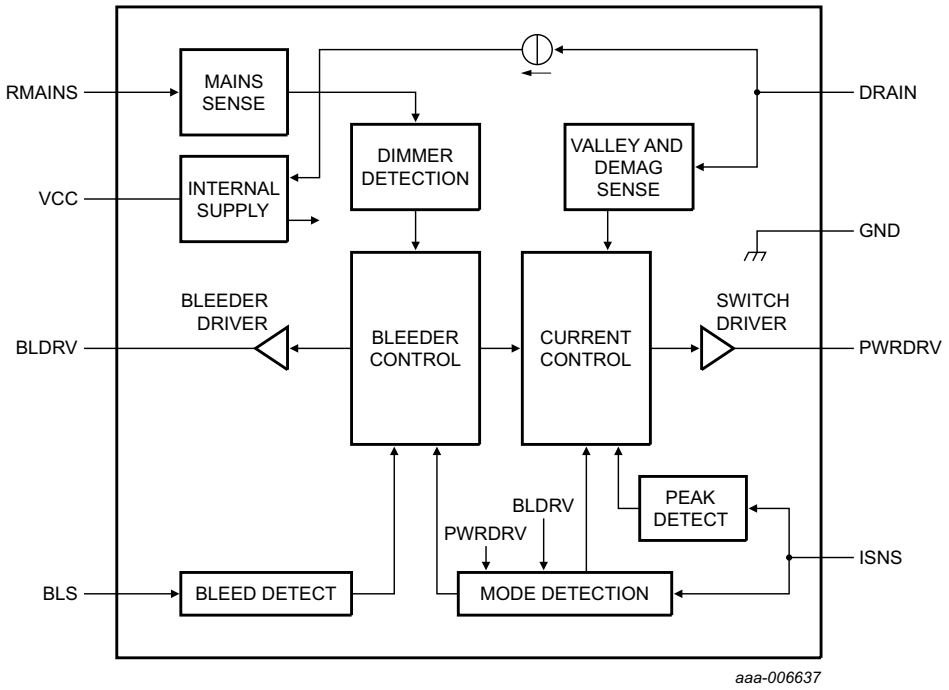

Fig 1. SSL5301T block diagram

7. Pinning information

7.1 Pinning

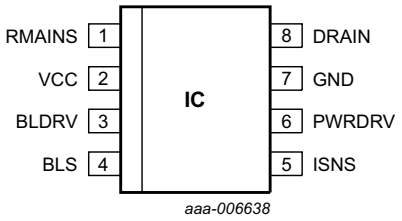

Fig 2. SSL5301T pinning diagram

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7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
RMAINS	1	mains detection input
VCC	2	IC supply input/output
BLDRV	3	bleeder stage transistor drive output
BLS	4	bleeder loop sense
ISNS	5	peak current sense input
PWRDRV	6	external MOSFET gate driver output
GND	7	ground
DRAIN	8	external MOSFET drain sense input

8. Functional description

8.1 Pin functionality

8.1.1 Pin RMAINS

The RMAINS pin takes in a current representing the rectified mains or dimmer output voltage via the external RMAINS resistors. The low ohmic input results in current always flowing, causing the voltage on the RMAINS pin to remain below the maximum $V_{i(RMAINS)}$ at any time.

The information about the mains voltage is used to set the dimming level and to shape the output current waveform in LTHD modes. It is also used for internal timing synchronizations, making it essential for low-ripple applications.

Some filtering may be required outside of the IC to eliminate incoming noise.

If the pin does not receive a rectified mains signal, the mains synchronization loss protection is triggered.

8.1.2 Pin VCC

At power-up, the VCC pin and its capacitor are charged using the internal HV current source from the DRAIN pin. Once V_{CC} has reached $V_{CC(startup)}$, switching starts and V_{CC} supply is generated from the auxiliary winding. If V_{CC} exceeds $V_{ovp(VCC)}$ due to, for example, a disconnected output, OVP is triggered. If V_{CC} drops to $V_{CC(low)}$, the internal HV current source is enabled. If V_{CC} drops below $V_{CC(stop)}$, UVLO protection is triggered.

Do not use the VCC pin to power additional circuitry outside the IC because no additional current budget is guaranteed. An additional V_{CC} load can affect product performance.

To support wall switches that include an indicator light, a predetermined current (I_{CC}) is pulled from the supply during a limited window of the VCC voltage (see condition 2 of I_{CC} in Table 7).

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8.1.3 Pin BLDRV

The BLDRV pin drives an external high-voltage NPN transistor stage. This stage is used to generate additional load current for a dimmer (see Section 8.2.6). Or it is used to load the mains during zero crossings when no dimmer is connected. It ensures proper mains detection. The voltage range is adapted to bipolar transistors only. At low BLDRV output voltage, the drive capability is reduced to limit current loss in case of bipolar transistor saturation.

8.1.4 Pin BLS

The BLS pin senses the total application current for dimmer compatibility (bleed sense, see Section 8.2.6).

Remark: A series resistor must be present between the BLS pin and the bleed loop sense resistor. The series resistor prevents that the current flowing out of the pin exceeds the limiting value, $I_{i(BLS)}$.

8.1.5 Pin ISNS

The ISNS pin senses the voltage across the sense resistor, R_{SNS}, generated by the inductor current flowing through the external MOSFET and this resistor (see Figure 3).

Optionally, a mode definition resistor is present between the pin and the current sense resistor. At start-up, the mode resistor is measured using a current which is sourced out of the pin.

8.1.6 Pin PWRDRV

The SSL5301T is equipped with a driver that controls an external MOSFET. The voltage on the driver output pin is increased towards the maximum $V_{o(PWRDRV)}$ to open the switch during the first cycle (t0 to t1; see Figure 4). It is pulled to ground from the start of the secondary stroke until the next cycle starts (t1 to t00). During the transition from low to high and back, the switching slope is controlled, limiting the high-frequency radiation.

8.1.7 Pin DRAIN

The DRAIN pin is used to derive energy to charge the VCC pin at start-up and after switching is stopped because of a triggered protection. The signal at the DRAIN pin is used to detect the occurrence of demagnetization. It is also used to determine the valley of the ringing voltage for starting the primary stroke.

8.2 Converter operation

8.2.1 Available modes

The SSL5301T incorporates various built-in operation modes which can be selected in the application using a maximum of three external resistors. At start-up, the value of these resistors is detected and the corresponding operation mode is set.

Mode resistors R_{TF} and R_{DIM} at the PWRDRV and BLDRV pins are connected between the pin and ground. Mode resistor R_{CTRL} at the ISNS pin is connected between the pin and the external MOSFET source (see Figure 3).

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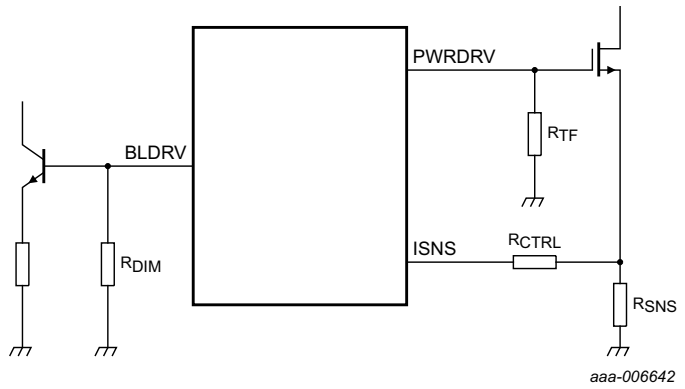

Fig 3. Mode resistor connections

Table 4 gives an overview of the available modes.

Table 4. Available modes

Parameter	How to set	Options	Mode resistor value
topology and frequency	R_{TF} on pin PWRDRV	flyback or buck-boost; HF mode	∞
		buck; HF mode	56 kΩ
		buck; LF mode	33 kΩ
		flyback or buck-boost; LF mode	15 kΩ
dim curve	R_{DIM} on pin BLDRV	curve 1; lin-log	10 kΩ
		curve 2; lin-log limited	∞
control mode	R_{CTL} on pin ISNS	low ripple (PF < 0.7)	0 kΩ to 0.5 kΩ or 3.3 kΩ
		eco-LTHD (PF ~ 0.75)	1.5 kΩ
		LTHD (PF > 0.9)	5.6 kΩ

8.2.2 Switching scheme

The converter in the SSL5301T is a Discontinuous Conduction Mode (DCM), peak current controlled system. When the output current control system requires a new switching cycle and the inductor current is zero, the external MOSFET is turned on at the next detected valley (see Section 8.2.3). The inductor current increases until a maximum, defined by the regulation loop, is reached and the external MOSFET is switched off. The inductor current reduces again. When the inductor current reaches zero, it is detected at the DRAIN pin. The detection enables the control system to regulate to an accurate average value of the LED current.

The maximum switching frequency can be set at two rates (see Section 8.2.1).

Three options are available which determine how the controller adjusts the maximum inductor peak current over the mains cycle. The result is either an optimal input current shape (optimized power factor and THD), a minimal LED current ripple, or an intermediate solution (eco-LTHD mode).

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8.2.3 Valley detection

A new cycle is started when the primary switch is switched on (see Figure 4). At a certain time (t1), the switch is switched off and the secondary stroke starts. After the secondary stroke (t3) has ended, the drain voltage shows oscillation or ringing. Circuitry at the DRAIN pin senses when the voltage on the drain of the switch has reached its lowest value (valley) during each oscillation. When the control loop requires the next cycle, it is started the next time a valley occurs. As a result, the capacitive switching losses reduce significantly. For successful valley detection, the frequency and amplitude of the drain voltage ringing must cause the slope of the ringing voltage to exceed the detection limit $(dV/dt)_{vrec}$ for at least $t_{d(vrec\text{-}swon)}$.

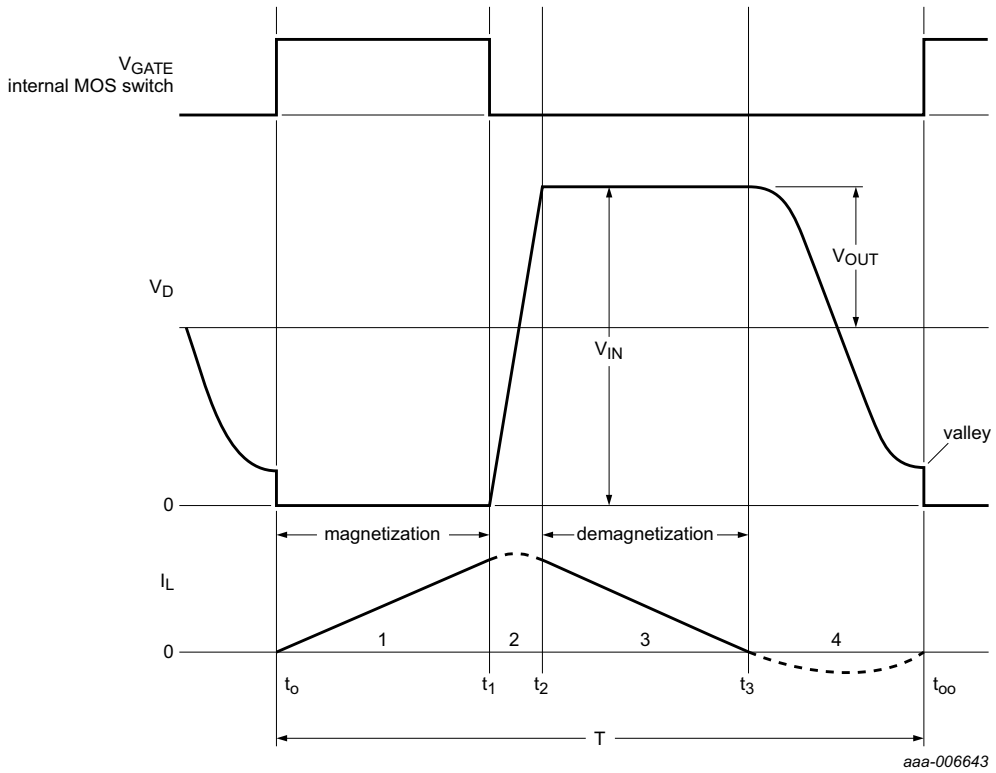

Fig 4. Buck waveforms and valley detection

8.2.4 Output current settings

The IC regulates the output LED current with great accuracy over line, load and component variations. The user can set the full-scale (100 %) value of the LED current. Choose a current sense resistor value, using Equation 1:

$$I_{LED} = \frac{V_{reg}}{R_{SNS}} \times N \quad (1)$$

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Where:

- V_{reg} is the set point of the internal regulation loop: 117 mV for LTHD buck-boost/flyback and 234 mV for LTHD buck and low ripple buck-boost/flyback, and 469 mV for low-ripple buck.
- R_{SNS} is the sense resistor on pin ISNS (see Figure 3)
- N is the transformer ratio.

The IC regulates the output current. It controls the current sense threshold voltage $V_{th(ISNS)}$, the number of switching cycles per (half-)mains period, and, if necessary, the switching frequency. The regulation depends on the mode of operation.

8.2.5 Preventing Continuous Conduction Mode (CCM)

To enable application design without having to include margins to ensure DCM operation, a CCM-prevention feature has been built in. The IC monitors the time gap between the end of the secondary stroke and the start of the next cycle. If this time becomes smaller than a predetermined idle time of about 1.8 μs, the controller reduces the switching frequency.

8.2.6 Dimming support

The SSL5301T can detect both leading edge and trailing-edge mains dimmer presence, as well as no dimmer presence at all. Support for smart dimmers that take additional supply current pulses is included. The phase information from the dimmer is translated to an LED output current level. To enable the application design for either optimal dimmer compatibility or limited bleeder power consumption, the following features are included:

- Bleeder stage support:

  The BLDRV pin is tailored to drive an external low-cost high-voltage NPN transistor, which creates a bleed current controlled by the SSL5301 internal control circuitry. The resulting bleed current is modulated over the mains phase to ensure correct dimmer operation

  - A strong bleed current is generated around the expected cutting edge of the dimmer output voltage. This edge is detected at the RMAINS pin. The NPN emitter resistor determines the maximum bleed current, given the maximum $V_{o(BLDRV)}$. An additional collector resistor can be added to distribute the bleeder stage power dissipation over its components. Reducing the current sourced at this pin according to its voltage level ($I_{source(high)BLDRV}$) limits current dissipation via the BLDRV pin.
  - A weak bleed current is generated to keep the dimmer in conduction when triggered. The generation of the weak bleed current is achieved when the total current to the dimmer is fed through a sense resistor R_{BLDSNS} (see Figure 5). The resulting voltage is measured at the BLS pin. A control loop in the IC uses this voltage to drive the external bleeder stage. The resulting bleeder current adds to the converter current so that the total current drawn by the application is kept constant.

    The regulation target voltage over R_{BLDSNS} equals $V_{th(reg)BLS}$.

    The reason for the additional resistor R_{PROT} is described in Section 8.1.4.

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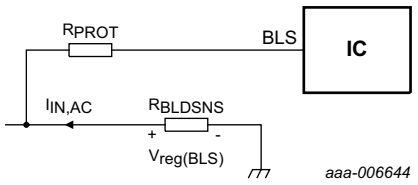


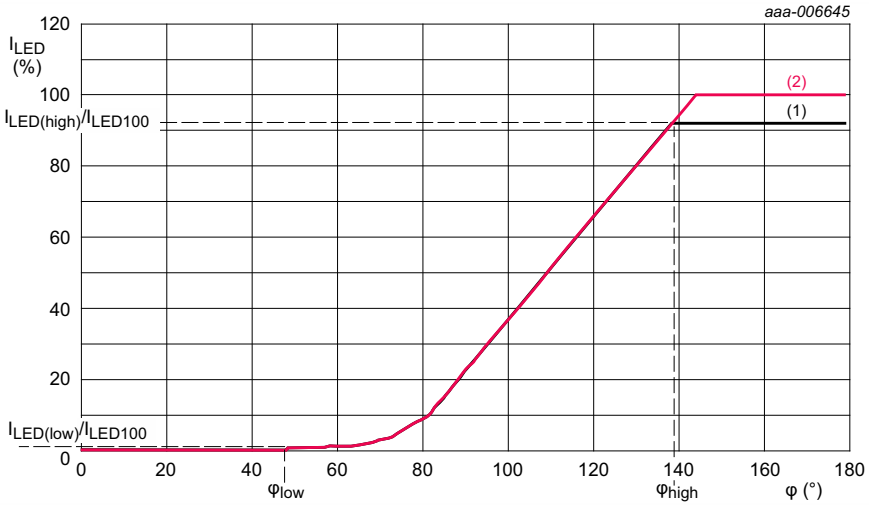
Fig 5. External components at the BLS pin

- Dimming curves:

  Two dimming curves are available to translate the detected dimmer phase to an output current level. $I_{LED(low)}/I_{LED100}$ gives the minimum output current level as a ratio of the full-scale current for either curve. The mode resistor at the BLDRV pin determines the selection (see Figure 6).

  – The lin-log curve has a smooth tail that matches human eye light sensitivity.

  – The lin-log limited curve enables optimal thermal lamp design. When no dimmer is detected, the output current is set to 100 %. When a dimmer is detected, the lin-log limited curve is used. The result is a lower maximum output current at a total power dissipation that equals the power dissipated when no dimmer is present.



(1) lin-log limited

(2) lin-log

Fig 6. LED current ratio as a function of dimmer phase angle

8.3 Protections

The IC incorporates the following protections:

- UnderVoltage LockOut (UVLO
- OverCurrent Protection (OCP)
- Brownout Protection
- Output Short Protection (OSP)

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- Output open OverVoltage Protection (OVP)
- Internal OverTemperature Protection (OTP)
- Mains synchronization loss protection
- Leading Edge Blanking (LEB)
- Bleeder dissipation protection

Output open OVP is a latched protection. Power-off cycling is required to exit the latched state. All other protections are not latched and lead to a safe restart of the converter.

8.3.1 UnderVoltage LockOut (UVLO)

When the voltage on the VCC pin drops below the value of $V_{CC(stop)}$, the IC stops switching. The internal HV current source is enabled. Once V_{CC} has increased to $V_{CC(startup)}$ the IC restarts after a minimum of 1 s back-off time.

8.3.2 OverCurrent Protection (OCP)

The SSL5301T contains a highly accurate peak current detector. It triggers when the voltage at pin ISNS reaches $V_{th(ISNS)}$. The circuit is activated after the leading edge blanking time (t_{leb}). There is a propagation delay between the peak current detection and the switch actually switching off. Due to this delay, the actual peak current is slightly higher than the peak current level set by the current sense resistor. The control loop compensates for this difference ensuring output current accuracy.

8.3.3 Brownout protection

The brownout protection is designed to limit the switch-on time in case of low input voltage. Because of the built-in peak current control, the input current otherwise slowly increases while no power is transferred to the output in a flyback configuration. The SSL5301T includes a maximum on-time of the switch $t_{on(high)}$.

8.3.4 Output short protection (OSP)

If, during the secondary stroke (switch-off time), a valley is not detected within the off-time limit ($t_{off(high)}$), the output voltage is typically less than the minimum limit allowed in the application. This condition can occur either during starting up or due to a short. A timer is started when $t_{off(high)}$ is detected, and is stopped only if a valid valley-detection occurs in one of the subsequent cycles. If no valley is detected for $t_{det(sc)}$, it is concluded that a real short-circuit exists and not a temporary start-up situation. The IC enters standby mode and tries to restart after a minimum of 9 s back-off time.

8.3.5 Output open OverVoltage Protection (OVP)

The result of an output open situation is that no power is delivered to the output, causing V_{CC} to increase and exceed $V_{CC(max)}$. Upon detection of this event, the IC enters the standby mode. The IC does not restart as long as mains voltage is present.

8.3.6 Internal OverTemperature Protection (OTP)

When the internal OTP function is triggered, the converter stops operating. This function is triggered at $T_{th(act)otp}$. The Overtemperature protection is an auto-restart protection. The IC restarts when the IC temperature drops below $T_{th(rel)otp}$.

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8.3.7 Mains synchronization loss protection

When the input current at the RMAINS pin fails to cross the "zero crossing detection" value of $I_{i(RMAINS)}$, no mains cycles are detected. If this situation persists for a time $t_{d(mld)}$, the IC stops switching. Once a valid mains signal is available again, the IC restarts.

8.3.8 Leading Edge Blanking (LEB)

A blanking time is implemented after switch-on to prevent premature detection of inductor peak current. At the opening of the MOSFET switch, a short current spike can occur because of the capacitive discharge of voltage over the drain and source. During the leading edge blanking time (t_{leb}), detection is disabled, so spikes are disregarded.

8.3.9 Bleeder dissipation protection

To limit dissipation in the bleeder, the dimmer detection state is limited to 16 mains half-cycles. If dimmer detection is not successfully completed, the IC restarts after a minimum of 9 s back-off time.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
General					
P_{tot}	total power dissipation	SO8 package	-	0.6	W
T_{amb}	ambient temperature		–40	+125	°C
T_j	junction temperature		–40	+190	°C
T_{stg}	storage temperature		–55	+150	°C
SR	slew rate	pin DRAIN	–10	+10	V/ns
Pin voltages and currents					
V_{CC}	supply voltage		–0.4	+34	V
$V_{i(RMAINS)}$	input voltage on pin RMAINS	current limited	–0.4	+5.2	V
$I_{i(RMAINS)}$	input current on pin RMAINS	at $V_{(RMAINS)}$ = 5.2 V	0	1	mA
$V_{i(BLS)}$	input voltage on pin BLS	current limited	–0.7	+5.2	V
$I_{i(BLS)}$	input current on pin BLS		–2.5	+2.5	mA
$V_{i(ISNS)}$	input voltage on pin ISNS		–0.4	+5.2	V
$V_{i(DRAIN)}$	input voltage on pin DRAIN	during mains surge; not repetitive	–0.4	+700	V
V_{ESD}	electrostatic discharge voltage	human body model [1]			
		all pins except pin DRAIN	–2000	+2000	V
		pin DRAIN	–1000	+1000	V
		charged device model [2]	–500	+500	V

[1] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Charged device model: equivalent to charging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

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10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; PCB: 2 cm × 3 cm; 2-layer; 35 μm Cu/layer	159	K/W
		in free air; PCB: JEDEC 2s2p	89	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	top package temperature measured at the warmest top of the case point	0.49	K/W

11. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High voltage						
$V_{I(DRAIN)}$	input voltage on pin DRAIN	[1]	-	-	675	V
$I_{i(DRAIN)}$	input current on pin DRAIN	JFET on strong; V_{DRAIN} = 675 V; V_{CC} = 17 V	4	5.5	7	mA
		JFET on weak; V_{DRAIN} = 675 V; V_{CC} < 4 V	500	550	600	μA
		JFET off; V_{DRAIN} = 675 V; V_{CC} = 20 V	-	-	15	μA
Supply						
$V_{CC(startup)}$	start-up supply voltage		17.5	18.5	19.5	V
$V_{CC(low)}$	low supply voltage	pin VCC	11.2	11.8	12.4	V
$V_{CC(stop)}$	stop supply voltage		8.8	9.3	9.8	V
$V_{CC(hys)}$	hysteresis of supply voltage	between $V_{startup}$ and V_{stop}	8.5	9.1	9.7	V
$V_{ovp(VCC)}$	overvoltage protection voltage on pin VCC		28	30	32	V
I_{CC}	supply current	pin DRAIN; V_{CC} < 4 V; standby mode	-	0.1	0.2	mA
		pin DRAIN; 4 V < V_{CC} < $V_{CC(low)}$; standby mode	1	1.25	1.5	mA
		pin DRAIN; V_{CC} > $V_{CC(low)}$; standby mode	-	0.2	-	mA
		pin VCC; normal operation, excluding drive currents to BLDRV and PWRDRV	-	2.25	-	mA

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Table 7. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Current regulator and protection						
f_{sw}	switching frequency	low-frequency mode; undimmed				
		50 Hz mains	55	60	65	kHz
		60 Hz mains	66	72	78	kHz
		high-frequency mode; undimmed				
		50 Hz mains	84	91	98	kHz
		60 Hz mains	101	109	117	kHz
$I_{LED(low)}/I_{LED100}$	low LED current ratio	[2]	-	0.008	-	-
$I_{LED(high)}/I_{LED100}$	high LED current ratio	lin-log limited curve; dimmer present [2]	-	0.92	-	-
φ_{low}	low phase		-	48	-	°
φ_{high}	high phase	lin-log curve	-	144	-	°
		lin-log limited curve	-	137	-	°
$V_{th(high)ISNS}$	high threshold voltage on pin ISNS	at peak current	1.195	1.24	1.285	V
$V_{th(low)ISNS}$	low threshold voltage on pin ISNS	(eco-)LTHD mode; at peak current	0.75	0.78	0.81	V
		low-ripple mode	0.33	0.35	0.37	V
t_{leb}	leading edge blanking time		-	600	-	ns
Valley detection						
$(\Delta V/\Delta t)_{vrec}$	valley recognition voltage change with time negative slope	voltage ringing on pin DRAIN	–26	–16	–6	V/µs
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time		-	100	-	ns
Brownout protection						
$t_{on(high)}$	high on-time	low-frequency mode				
		50 Hz mains	13.2	14.4	15.6	µs
		60 Hz mains	11.0	12.0	13.0	µs
		high-frequency mode				
		50 Hz mains	8.8	9.6	10.4	µs
		60 Hz mains	8.3	9.0	9.7	µs
Output short protection						
$t_{off(high)}$	high off-time		32	40	48	µs
$t_{det(sc)}$	short-circuit detection time	50 Hz mains	10	-	20	ms
		60 Hz mains	8.3	-	16.7	ms
Temperature protections						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature	on-chip	160	175	190	°C

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Table 7. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(rel)otp}$	overtemperature protection release threshold temperature	on-chip	90	102	114	°C
Pin PWRDRV						
$V_{o(PWRDRV)}$	output voltage on pin PWRDRV	high level				
		$V_{VCC} > V_{CC(low)}$	-	10.7	-	V
		$V_{VCC} = V_{CC(stop)}$	-	8.5	-	V
$I_{source(PWRDRV)}$	source current on pin PWRDRV	20 μs maximum; V_{PWRDRV} = 2 V	-	360	-	mA
$I_{sink(PWRDRV)}$	sink current on pin PWRDRV	20 μs maximum; V_{PWRDRV} = 10 V	-	900	-	mA
		20 μs maximum; V_{PWRDRV} = 2 V	-	260	-	mA
Pin BLDRV						
$V_{o(BLDRV)}$	output voltage on pin BLDRV	high level				
		near mains zero crossings	0.92	0.95	1.00	V
		strong bleeding	2.87	3.05	3.18	V
		weak bleeding	1.8	1.9	2.0	V
$I_{source(BLDRV)}$	source current on pin BLDRV	$V_{o(BLDRV)}$ = 0.25 V	0.3	-	0.9	mA
		$V_{o(BLDRV)}$ = 0.95 V	1.2	-	2.3	mA
		$V_{o(BLDRV)}$ = 2.9 V	3.9	4.4	4.9	mA
$I_{sink(BLDRV)}$	sink current on pin BLDRV	$V_{o(BLDRV)}$ = 0.4 V	85	115	145	μA
Pin BLS						
$V_{reg(BLS)}$	regulation voltage on pin BLS	dimmer detected	-	−0.327	-	V
Pin RMAINS						
$I_{i(RMAINS)}$	input current on pin RMAINS	at top of mains sine wave	324	360	396	μA
		for zero cross detection	18	22.5	27	μA
$t_{d(mld)}$	mains loss detection delay time	50 Hz mains; no dimmer	-	60	-	ms
		50 Hz mains; dimmer	80	-	160	ms
		60 Hz mains; no dimmer	-	50	-	ms
		60 Hz mains; dimmer	67	-	133	ms
$I_{sink(RMAINS)}$	sink current on pin RMAINS	$V_{i(RMAINS)}$ = 4 V	400	-	-	μA

[1] The peak voltage on pin DRAIN occurs each switching cycle, based 25,000 hours device lifetime.

[2] Actual LED current values are slightly lower due to the IC supply current. If the AUX supply is unable to support the IC supply current, the control loop increases the low LED current limit.

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12. Application information

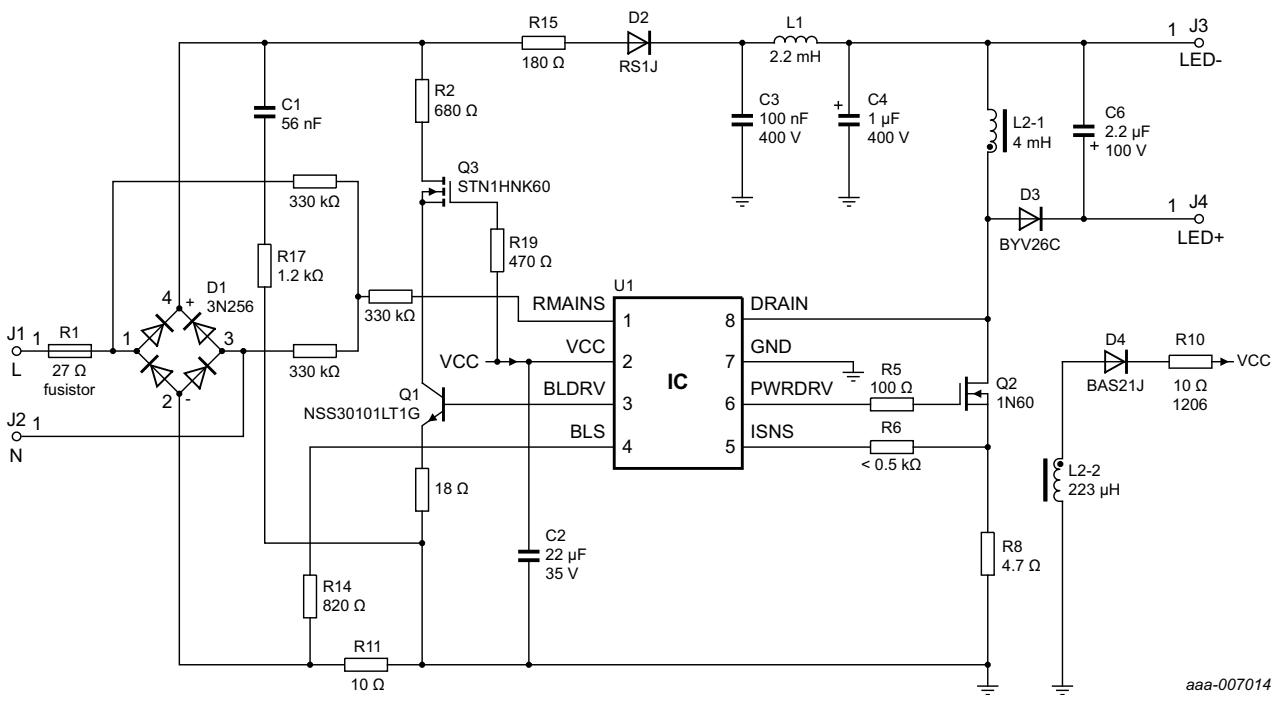

Fig 7. SSL5301T buck-boost configuration; low ripple; input = 230 V (AC); output = 90 V/50 mA

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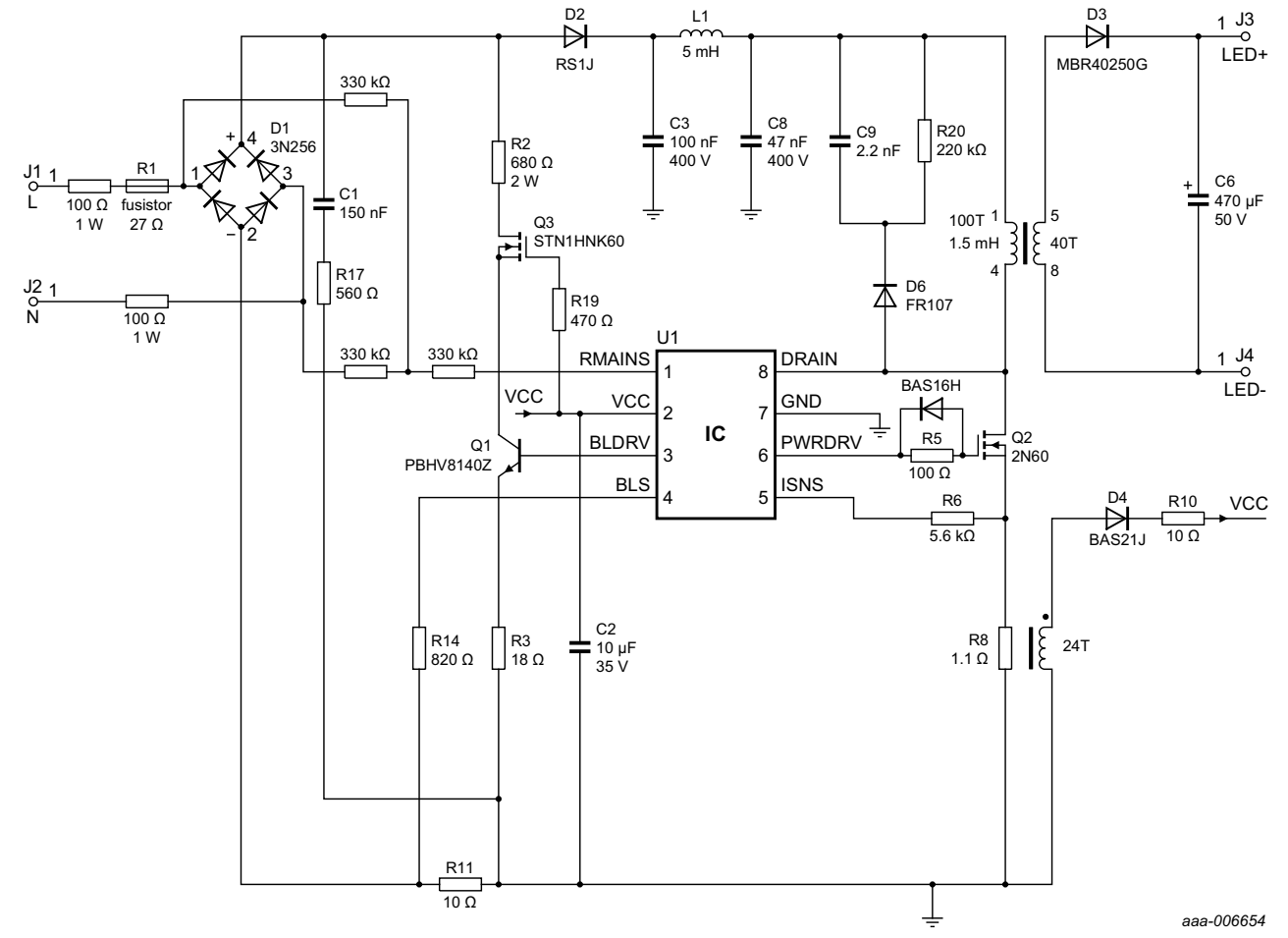

Fig 8. SSL5301T flyback configuration; low THD; input = 230 V (AC); output = 36 V/250 mA

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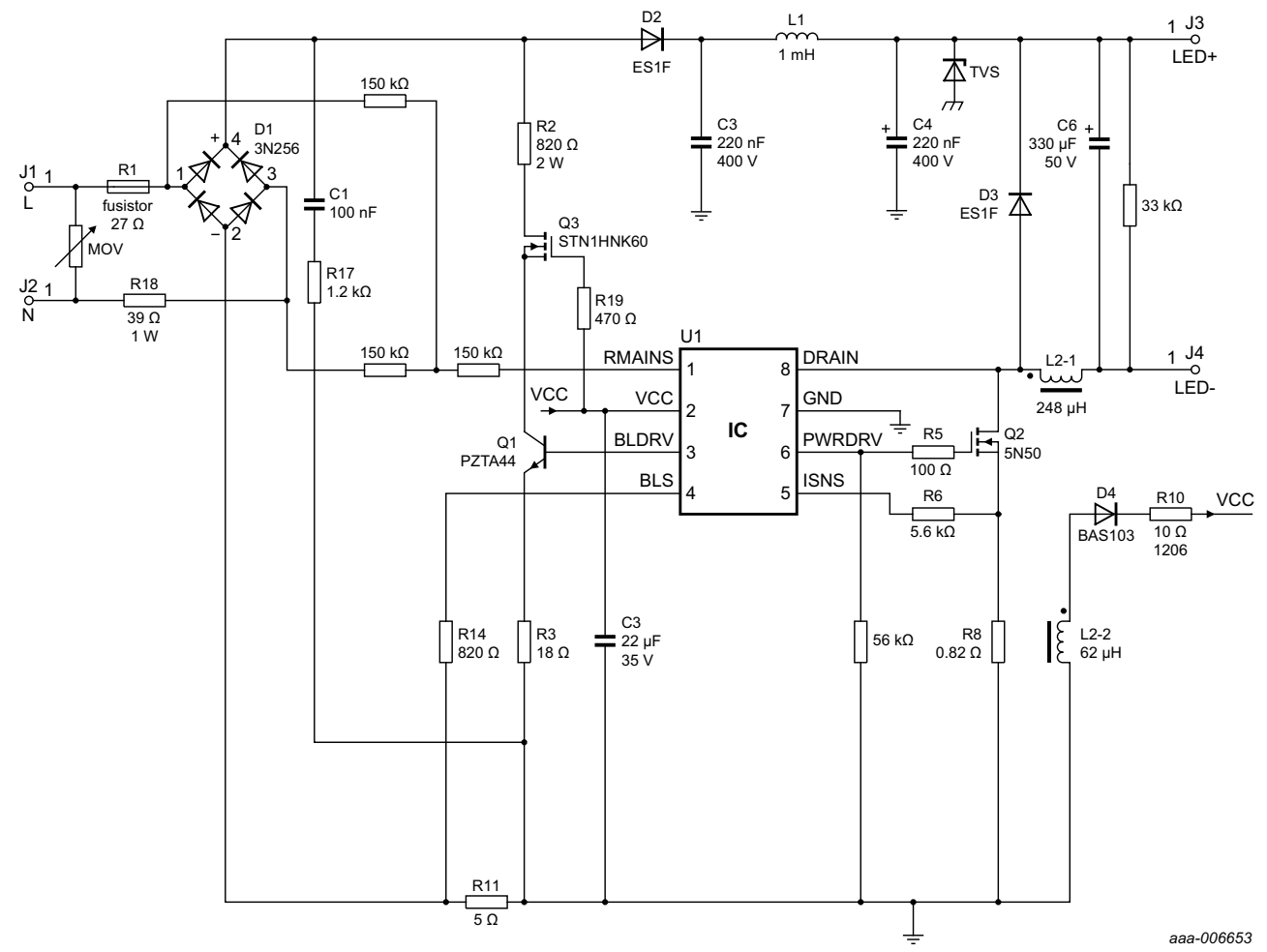

Fig 9. SSL5301T buck configuration; low THD; input = 120 V (AC); output = 37 V/290 mA

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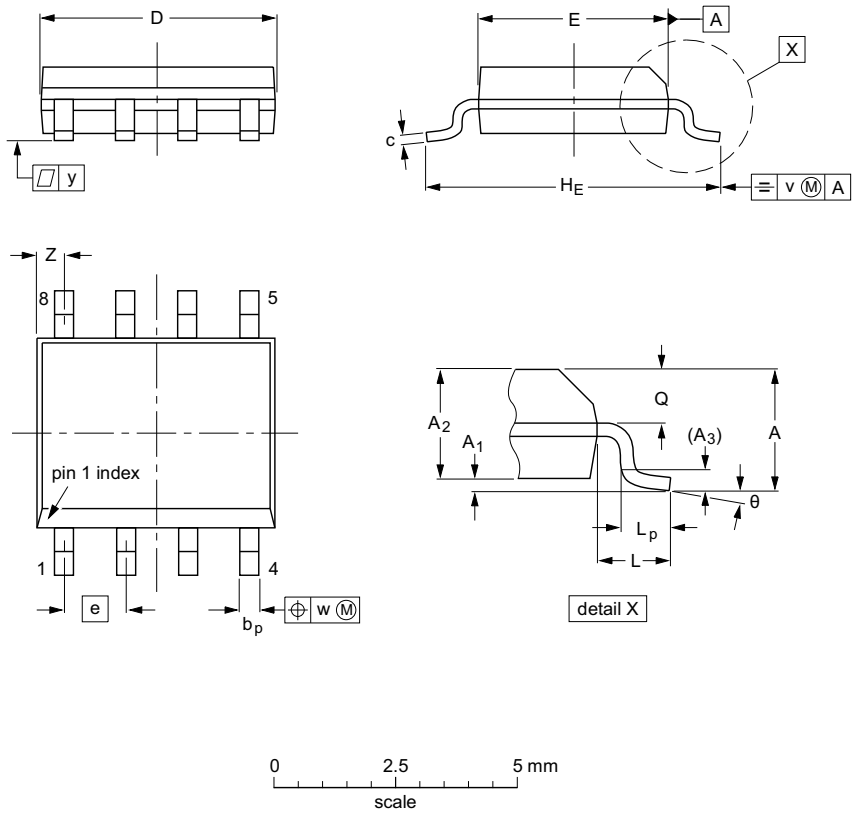
13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 10. Package outline SOT96-1 (SO8)

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14. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSL5301T v.2	20140630	Product data sheet	-	SSL5301T v.1
Modifications:	• Data sheet status has changed from Preliminary to Product. • Text and graphics updated throughout the document.			
SSL5301T v.1	20140602	Preliminary data sheet	-	

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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